STATUS OF THE CLAIMS

The status of the claims of the present application stands as follows:

1. **(Currently Amended)** A method of reducing the magnitude of an overall instantaneous current draw during a timing cycle in a synchronous integrated circuit having a plurality of timing paths each having a late mode margin associated therewith, comprising the steps of:
   (a) stepping through the plurality of timing paths so as to ~~determining~~ determine for each one of the plurality of timing paths whether or not the corresponding late mode margin is greater than zero;
   (b) in response to the corresponding late mode margin being determined to be greater than zero in step (a), adding a ~~corresponding~~ delay to the corresponding one of said plurality of timing paths; and
   (~~b~~c) in response to the corresponding late mode being determined to be greater than zero in step (b), inserting a delay element into ~~each~~ the corresponding one of the plurality of timing paths ~~having said corresponding delay~~, said delay element configured to induce said ~~corresponding~~ delay into that one of the plurality of timing paths.

2. **(Currently Amended)** A method according to claim 1, wherein at least some of the plurality of timing paths each have early mode problems, the method further comprising, prior to step (~~b~~c), the step of fixing said early mode problems.

3. **(Currently Amended)** A method according to claim 1, wherein each one of the plurality of timing paths has a corresponding late mode margin and step (a~~b~~) includes setting each said ~~corresponding~~ delay to said corresponding late mode margin.

4. **(Currently Amended)** A method according to claim ~~3~~1, wherein ~~the overall instantaneous current draw has a profile and~~ each one of the plurality of timing paths has a corresponding late mode margin and step (a~~b~~) includes setting each one of at least some of said ~~corresponding~~ delays to said corresponding late mode margin minus a fraction of the timing cycle.

5. **(Currently Amended)** A method according to claim 4, wherein at least some of the plurality of timing paths each have early mode problems, the method further comprising, ~~following~~ prior to step (~~a~~c), the step of fixing said early mode problems.

6. **(Currently Amended)** A method according to claim 3, wherein each one of the plurality of timing paths has a corresponding early mode margin and step (~~a~~b) includes setting each ~~corresponding~~ delay to said corresponding late mode margin minus said corresponding early mode margin.

7. **(Currently Amended)** A method according to claim ~~6~~1, ~~wherein the overall instantaneous current draw has a profile and step (a) includes setting each one of at least some of said corresponding delays to said corresponding late mode margin minus a fraction of the timing cycle~~ wherein the overall instantaneous current draw has a profile having a peak defined by a portion of the plurality of timing paths, the method further comprising the step of removing at least one timing path from said portion of the plurality of timing paths.

8. **(Currently Amended)** A method according to claim 7, wherein at least some of the plurality of timing paths each have at least one early mode problem, the method further comprising, ~~following~~ prior to step (~~a~~c), the step of fixing said early mode problems.

9. **(Currently Amended)** A method of reducing the magnitude of an overall instantaneous current draw during a timing cycle in a synchronous integrated circuit having a plurality of timing paths each having a late mode margin, the instantaneous current draw having a profile that includes a peak defined by a portion of the plurality of timing paths, comprising the steps of:

(a) determining if the late mode margin of each one of the plurality of timing paths is greater than zero; ~~and~~

(b) for each one of the plurality of timing paths having a late mode margin greater than zero, determining a delay for that one of the plurality of timing paths in direct response to the determination of step (a), said delay being a function of the corresponding late mode margin; and

(c) removing at least one timing path from said portion of the plurality of timing paths.

10. **(Original)** A method according to claim 9, wherein each said delay is equal to the corresponding late mode margin.

11. **(Canceled)**

12. **(Currently Amended)** A method according to claim 9, wherein at least some of the plurality of timing paths each have at least one early mode problem, the method further comprising the step of fixing each one of said ~~late~~ early mode problems.

13. **(Canceled)**

14. **(Original)** A method according to claim 9, wherein the plurality of timing paths each have an early mode margin, the method further comprising the step of, for each one of the timing paths having a late mode margin greater than zero and an early mode margin greater than zero, subtracting the early mode margin from the late mode margin.

15. **(Canceled)**

16. **(Currently Amended)** An integrated circuit, comprising:

(a) a plurality of timing paths ~~each having a late mode margin~~ resulting in a timing cycle histogram; and

(b) ~~a delay element located in each one of at least some of said plurality of timing paths, each of said delay elements having a delay that is a function of said late mode margin of the corresponding one of said plurality of timing paths~~a plurality of delay elements distributed among said plurality of timing paths in response to redistributing at least some of said plurality of timing paths within said timing cycle histogram.

17. **(Original)** An integrated circuit according to claim 16, wherein each said delay is substantially equal to said late mode margin of the corresponding one of said plurality of timing paths.

18. **(Original)** An integrated circuit according to claim 16, wherein at least one said delay is substantially equal to said late mode margin of the corresponding one of said plurality of timing paths minus a predetermined period.

19. **(Original)** An integrated circuit according to claim 16, wherein said plurality of timing paths each have an early mode margin and each said delay is substantially equal to the difference between said late and early mode margins of the corresponding one of said plurality of timing paths.

20. **(Original)** An integrated circuit according to claim 16, wherein at least one said delay is substantially equal to the difference between said late and early mode margins of the corresponding one of said plurality of timing paths minus a predetermined period.